REMARKS

Claims 1-5 and 7-13 are pending in the application. Claims 1, 8, 12, and 13 have been amended and claims 14-26 have been added, leaving claims 1-5 and 7-26 for consideration upon entry of the present Amendment. Support for the amendment can be found in Figures 7, 9A, 9B, and 10, and the corresponding description in the specification. Applicants respectfully request reconsideration in view of the Amendment and Remarks submitted herewith.

The Examiner has objected to the drawings under 37 CFR 1.83(a). The Examiner asserts that the drawings do not show a first electrode being absent from at least the drive circuit region. Figure 7 has been amended to reflect the claimed limitation. Support for the amendment can be found on page 15, lines 13-19. In particular, Figure 7 has been revised so that the single-dot broken line specifically surrounds the drive circuits. Accordingly, Applicants respectfully request that this objection be withdrawn.

Claims 1-5, 7-26 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamada et al. (US 6,072,450) in view of Applicant's admitted prior art, figure 1. For an obviousness rejection to be proper, the Examiner must meet the burden of establishing that all elements of the invention are disclosed in the prior art; that the prior art relied upon, coupled with knowledge generally available in the art at the time of the invention, must contain some suggestion or incentive that would have motivated the skilled artisan to modify a reference or combined references; and that the proposed modification of the prior art must have had a reasonable expectation of success, determined from the vantage point of the skilled artisan at the time the invention was made. *In re Fine*, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988); *In Re Wilson*, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970); *Amgen v. Chugai Pharmaceuticals Co.*, 927 U.S.P.Q.2d, 1016, 1023 (Fed. Cir. 1996).

The Examiner acknowledges that Yamada does not disclose a peripheral driving circuit and a common cathode being absent from the driving circuit. The Examiner also asserts that Yamada does not teach integrating circuits on the same substrate as the pixel section. The Examiner also asserts that Applicant's Figure 1 discloses a peripheral drive circuit. The Examiner then concludes that when combining these teachings that it would have been obvious that the common cathode would not be formed in the peripheral driving circuit region as well. Applicants respectfully traverse.

First, Applicants note that the Examiner has not pointed to any references that teach that the common cathode would not be formed over the entire substrate. Moreover, the claims recite a specific location of the first electrode and/or cathode on the substrate. In particular, all of the claims recite that there are two regions: (1) a display pixel region; and (2) a peripheral region, which has a peripheral drive circuit, or a peripheral drive circuit region (both terms hereinafter referred to as the "peripheral drive circuit region"). All of the claims also recite that said first electrode and/or cathode overlaps the display pixel region, terminates in a substrate region on the inside the peripheral drive circuit region, and is absent from the peripheral drive circuit region. The Examiner has not pointed to any reference that teaches or suggests that limitation.

Moreover, when one skilled in art forms the display pixel region and the peripheral drive circuit region, those skilled in the art would normally form the first electrode to overlap substantially the entire surface of the substrate, thereby overlapping both the display pixel region and the peripheral drive circuit region. The feature of forming the first electrode to overlap only the pixel region and to terminate so as to avoid overlapping the peripheral drive circuit region located outside the display pixel region is not taught in any references and thus is not obvious.

As further evidence that one skilled in art would have only formed the first electrode so as to cover both the display pixel region and the peripheral drive circuit region, Applicants submit herewith JP Laid-Open Publication No. Hei 11-024606 (hereinafter referred to as the JP '606 publication), laid open in Japan on January 29, 1999. Applicants are also submitting U.S. 6,618,029, as the English translation of the JP '606 publication. Applicants note that U.S. 6,618,029 is not prior art against the application. The JP '606 publication clearly shows that those skilled in the art would normally form the common first electrode to overlap both the pixel region and the peripheral drive circuit region when employing the configuration of forming the pixel region and the drive circuits on the same substrate.

For example, in Figs. 8(G) and 12(B) of the JP '606 publication, a second interlayer insulation film 52 is formed over the TFTs 20, 30 provided for each pixel, and an emissive element 40 is further formed on top. The uppermost counter electrode op of this element is formed in common for a plurality of pixels.

Paragraph [0048] of the JP '606 publication describes that "the counter electrode op is formed to overlap at least the pixel region on the entire surface or in stripes * * * ." Further, paragraph [0052] recites as follows: "Both the data side drive circuit 3 and the scan side drive

circuit 4 are covered by a bank layer. Accordingly, although the counter electrode op may overlap the drive circuit region, the bank layer serves to intervene between the wiring layer of the drive circuits and the counter electrode op. This prevents parasitic capacitance from generating in the drive circuits 2, 3, reducing load of the drive circuits 2, 3. With this arrangement, reduced power consumption or a higher display operation speed can be achieved."

Furthermore, as also can be seen in Fig. 1, the region in which the bank layer is formed is explained in paragraph [0048] as follows: "the bank layer is formed with respect to the entire peripheral region of the transparent substrate 10 shown in Fig. 1." In other words, the bank layer for intervening between the drive circuits and the counter electrode op is formed over the entire region of the substrate 10. The purpose of providing this bank layer is, as noted above, to prevent generation of parasitic capacitance between the drive circuits and the counter electrode op. From this, it can be understood that, in the JP '606 publication, the region in which the bank layer is formed corresponds to the region in which the counter electrode op is formed. It is therefore apparent that the counter electrode op is formed in substantially the entire bank layer region on the substrate, covering the drive circuits 3, 4 and 5 disposed in the peripheral region of the substrate 10.

In the JP '606 publication, a black resist material is used as the bank layer. The bank layer is thick and insulative, as is apparent from its purpose and the illustrations in the drawings. While the bank layer is formed on the entire surface of the substrate 10, the bank layer is intentionally removed from the area in which a mounting pad 6 is arranged in an end portion of the substrate 10. The mounting pad 6 serves to achieve electrical contact with an external power source or the like. It is obvious to those skilled in the art that, in the area of the mounting pad, formation of a thick insulation film such as the bank layer in addition to the interlayer insulation film should be avoided so as to ensure electrical conduction. In the JP '606 publication, in the final state, the bank layer is absent from the area of the mounting pad 6. However, because it is impractical to partially avoid depositing a bank layer composed of a resist material, it is apparent to those skilled in the art that the bank layer is intentionally removed after being deposited in the area of the mounting pad 6.

From the point of view of the mounting pad 6, such formation and removal of the thick bank layer may cause a contact failure due to an etching failure or oxidation of the pad (metal) surface resulting from exposure to an etching solution. Regardless of such risks, the bank layer

is formed on the entire substrate surface in the JP '606 publication. From this fact, it is apparent that the counter electrode op is formed on the entire substrate surface including the region over the drive circuits 3, 4 and 5.

In other words, as can be seen in the JP '606 publication, even when the drive circuits are formed on the same substrate as the pixel region, it was a normal understanding for those skilled in the art at the time of conceiving the present invention to form the common counter electrode op to overlap not only the pixel region but the entire substrate. Further, the prior art documents nowhere mention or suggest terminating the common electrode on the inside of the substrate peripheral region in which the drive circuits are arranged.

When the emissive element includes an organic compound in its emissive layer as in the present invention, the low resistance of the organic compound with respect to moisture and oxygen is a significant problem. It was therefore important for those skilled in the art at the time of conceiving the present invention to reduce as much as possible the probability that moisture and oxygen enters into the emissive layer from outside. Accordingly, as described in the "related art" in the present application, the common knowledge among those skilled in the art is that an electrode formed in an upper layer of the emissive layer (the counter electrode op in the JP '606 publication) is to be formed on the entire substrate surface.

As explained above, even when the drive circuits are formed on the same substrate as the pixel region, it is the common knowledge among those skilled in the art that a common electrode is to be formed over substantially the entire surface of the substrate. By combining such prior art with Yamada, which nowhere mentions or suggests integrating the pixel region and the peripheral drive circuit on the same substrate, the resulting configuration is simply that of the "related art" described in the present application. The configuration disclosed in the JP '606 publication is also substantially identical to that of the "related art." Moreover, based on Yamada and the JP '606 publication, formation of the common first electrode in a pattern which overlaps the pixel electrode while terminating so as to avoid overlapping the peripheral drive circuit region integrated on the same substrate on the outside of the pixel region, as in the present invention, cannot be obvious, because no motivation for devising the configuration of the present invention can be found. As such, the present invention is not at all obvious from Yamada and other references.

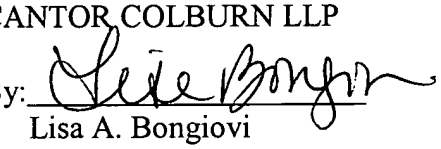
Applicants also incorporate and maintain all of the arguments made in the response filed on February 28, 2003.

In view of the foregoing, it is respectfully submitted that the instant application is in condition for allowance. Accordingly, it is respectfully requested that this application be allowed and a Notice of Allowance issued. If the Examiner believes that a telephone conference with Applicants' attorneys would be advantageous to the disposition of this case, the Examiner is cordially requested to telephone the undersigned.

In the event the Commissioner of Patents and Trademarks deems additional fees to be due in connection with this application, Applicants' attorney hereby authorizes that such fee be charged to Deposit Account No. 06-1130.

Respectfully submitted,

CANTOR COLBURN LLP

By: 

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